European Heterogeneous Cloud / Edge infrastructure for Next Generation Hybrid Services

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Digital Sovereignty as an Engineering Problem for Cloud and Edge Servers: Open Standards and Interfaces in the HIGHER Project

Webinar hosted by HiPEAC [https://hipeac.net/webinars/]

October 29th, 2026

Digital Sovereignty is mostly debated as policy

- … the most frequent concerns being:
  - Jurisdiction, Data location, Procurement rules, Certification
  - All necessary concerns, but none of them reach the actual systems.
- Position: Sovereignty is to be decided in specifications.
  - Can a data centre (DC) server be specified end to end, on open standards, by parties who can be held accountable for it ?
- Highlights of critical underlying supply chain dependencies:
  - Instruction Set Architecture ← is licensed from elsewhere
  - Firmware (esp. board control) ← unauditable
  - Conventions for rack systems (mechanical/thermal/management) ← defined by consortia and hyperscalers that European projects join late, if at all

Sovereign services on machines that no European party has specified ?!

Policy claims lacking a solid engineering basis …

Digital Sovereignty as an Engineering Question

- Can a data centre (DC) server be specified end-to-end, on open standards, by people who can be held accountable for it ?
- The operative test is maintaining visibility and influence into specifications, together with accountability.
- Clauses on “Ownership”, “manufactured in Europe”, “exclusion of non-European parts” are not enough.
- 3 main domains, but no single one answers the question above.
  - Processor design, Data-centre production, Software ecosystem



3 Different “Clock Domains”

Research and processor design

DEVELOPMENT CADENCE

3–4 years

project cycle, proposal to final review

EXPECTED LIFETIME

10+ years

ratified ISA and IP blocks outlive the project

INCENTIVE

novelty, demonstration, publication

Data centre production and supply chain

DEVELOPMENT CADENCE

2–3 years

platform programme, design to deployment

EXPECTED LIFETIME

5–8 years

System boards in service before decommissioning

INCENTIVE

volume, cost, conformance

Software ecosystem and operations

DEVELOPMENT CADENCE

9–10 weeks

upstream kernel release cadence

EXPECTED LIFETIME

15+ years

an upstream driver outlives the hardware it was written for

INCENTIVE

installed base, support burden

The fastest cadence (== SW) carries the longest commitment → upstreaming early is imperative.

Proposed approach: 3 Bridges

- Research prototypes to track industrial supply chains
  - Conform to standards nobody in the project invented.
  - Document and specify for integrators, not for reviewers.
- Open ISA standards to be carried into open rack-scale standards
  - Break the circular dependency bet. hardware & software: (1) Put HW in the hands of SW developers before it is a product. (2) Upstream early, on a continuous basis.
- Place European designs (silicon, platform) in context with global standards
  - Open Compute Project (OCP), RISC-V International, PCI-SIG / CXL, DMTF.
  - Organizations: UEFI Forum, TCG (TPM, DICE, DPE), SSI, JEDEC, SNIA, UALink/UltraEthernet.



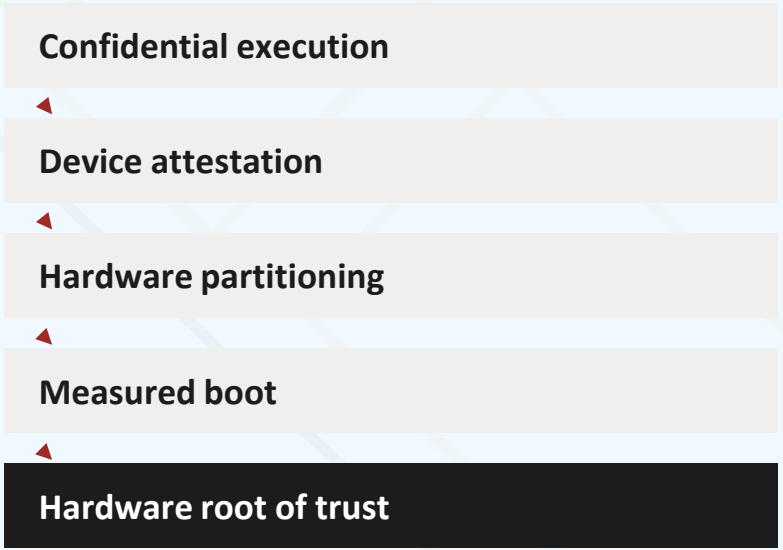


Composition & Dependability

A server placed near industrial processes or critical infrastructure acts on the physical world and is assembled from parts of many origins. It cannot be trusted by assertion.

> *Openness is what makes trust auditable rather than asserted. That is the crux of the engineering argument for open standards.*

A VERIFIABLE CHAIN, FROM SILICON UPWARD



Lessons learnt from RISER & HIGHER

RISER

European RISC-V silicon of the EPI / EUPilot lineage, on boards conforming to mainstream I/O and storage standards. Open-source stack, two deployment models (accelerator, microserver).

Established: research silicon can take a form a data centre recognises.

HIGHER

Arm and RISC-V side by side. OCP-aligned management and firmware. Platform RoT as security anchor. Disaggregated memory over CXL. Deployment on cloud racks through to edge nodes.

Extends RISER: from a board that boots to a platform that can be operated and attested.

Crucial concerns exposed by both projects

Availability of critical IP blocks · Software readiness · Discontinuities between the sources (financial instruments) that supplied the silicon, funded integration, and govern the standards the results must reach.

RISER (2023-2026) - "RISC-V for cloud services". Horizon Europe, Grant Agreement: 101092993

HIGHER (2024-2027) - "European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services". Horizon Europe, Grant Agreement: 101189612

What needs to be specified end-to-end ?

(shading used to show areas where European presence/influence is weaker)

	open standards & interfaces
Workloads — cloud services, edge and industrial applications, containers	OCI image / runtime
Orchestration — cloud-native stack, MetaOS	Kubernetes CRI / CNI / CSI **ColonyOS** (MetaOS)
System software — OS (Linux, MetaOS, RTOS), hypervisor, drivers, toolchains	UEFI, ACPI, **OpenSBI**, **RVA23**
Platform management firmware, auditable boot path	OCP **DC-SCM**, **Caliptra** (PRoT), TPM, DMTF SPDM / Redfish
Rack and facility conventions — mechanical, thermal, power	OCP ORV3 (racks & power distr), **DC-MHS** (modular HW)
Server boards — OCP HPM / DC-SCM, PCIe, NVMe, CXL, high-performance NICs	OCP **HPM**, **PCIe**, **CXL**, NVMe, OCP NIC
Silicon and IP — European processors; Arm and RISC-V ISAs	**RISC-V** ISA + CoVE / IOPMP / Smmtt, **DICE**, Armv9-A, **Arm BSA**

A point of tension: design/development (+ funding) has run ahead of the standards work.

+ TCG DICE Protected Environment (DPE)

+ provenance (esp. SBOM) across every layer (SPDX ISO/IEC 5962 / CycloneDX)

Conclusion

- Feasibility is no longer the principal uncertainty.
- An open call to action:
  - Edge & industrial deployment scenarios that genuinely stress sovereign platforms
  - Dependability and certification expertise, esp. developing the people who know what an assessor asks for
  - Integrators working in alignment with DC supply chains (esp. OCP)

My take: In Europe, we can already design & build DC platforms, but cannot yet supply the deployment context, market pull (first customer), or the certification flow on our own.



Thank you for your attention.



https://higher-project.eu

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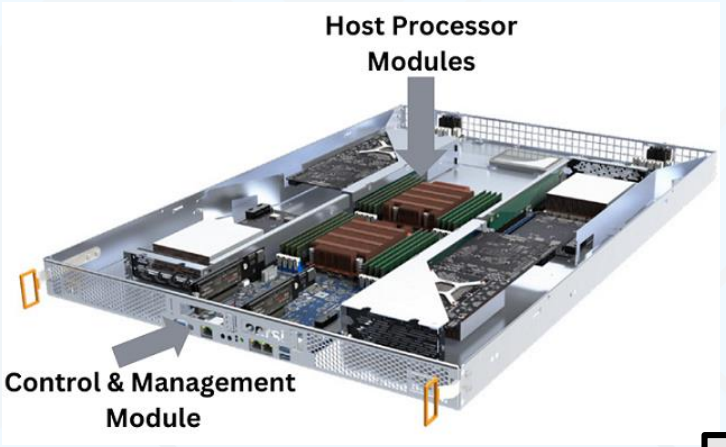
The HIGHER Roadmap

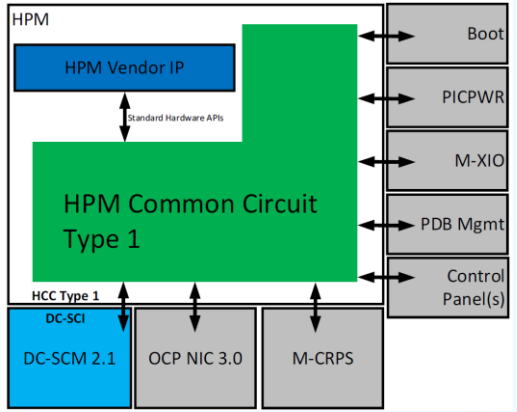
European Heterogeneous Cloud/Edge Infrastructures for Next Generation Hybrid Services

Objectives:

- Cloud and edge HW and SW modules based on European Technologies, demonstrating full computing infrastructure deployments
- Processing and Energy efficiency able to satisfy the needs of demanding cloud and edge applications

- Open Compute Project → "recipes" for data-centre systems
- HIGHER → Data-centre ready processor (Arm, RISC-V) & management modules based on OCP (HPM, DC-SCM)

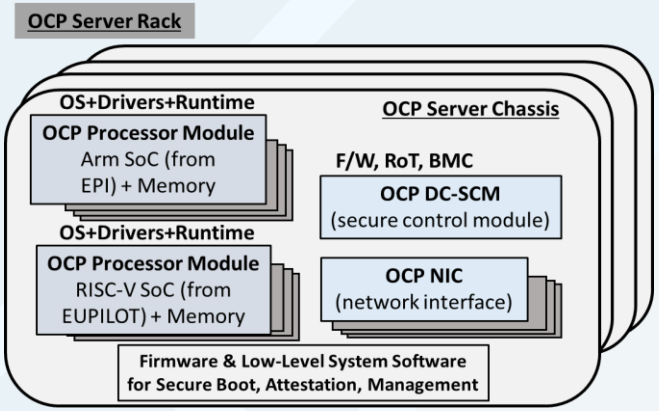


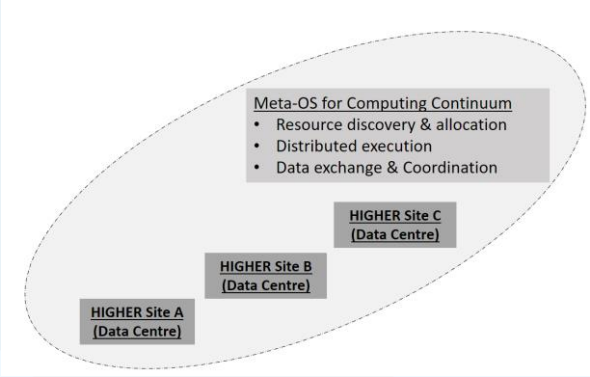


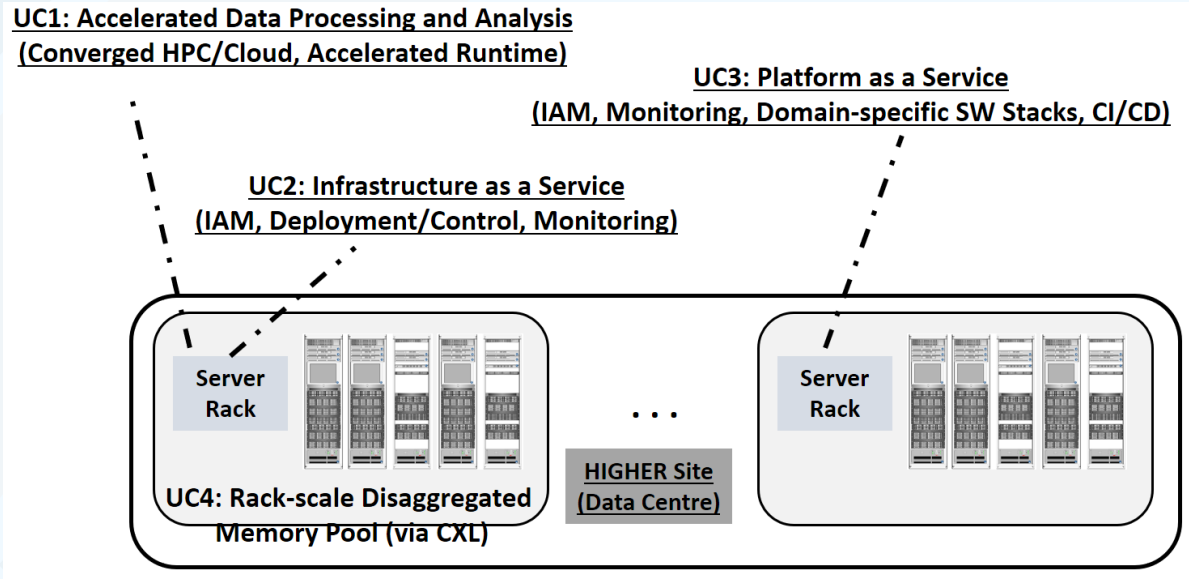
HIGHER (GA 101189612 - DG/Agency: HADEA): https://higher-project.eu
Call: HORIZON-CL4-2024-DIGITAL-EMERGING-01-CNECT

Key themes: Cloud, Edge, Computing Continuum, ARM, RISC-V, Data Centre Computing, Open Source Software

Technology & Use-Cases in HIGHER







Approach: *Overall, HIGHER will develop novel, mostly open-source, hardware and software modules and systems leveraging technologies developed, among others in the EPI and EUPilot projects, as well as standards established by the Open Compute Project (OCP), enabling the deployment of complete modular open cloud and edge infrastructures. HIGHER will further adopt a socket-based approach for EPI and EUPilot processor chips aiming at developing an EU socket reference, enabling interoperability and smooth processor upgrades.*